REMARKS

The Examiner's final Office Action mailed on December 10, 2002 has been received and its contents carefully considered.

Claims 21-27 and 42-52 are pending in this application. Claim 44 is amended herein. The changes are shown in the marked-up version of claim 44 appended to this Amendment. The title of the invention is also revised herein. Consideration and entry of this Amendment pursuant to 37 CFR §1.116 is respectfully requested.

In the final Action, the Examiner objected the title of the invention as not descriptive. The title is revised herein to be more clearly indicative of the invention to which the claims are directed. Approval of the new title proposed by the applicant is respectfully requested.

The Examiner rejected claims 21-41 and 42-52 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Specifically, regarding claims 21-22 and 44-45, the Examiner asserts it is not clear what item is "dividing the wafer into a plurality of semiconductor devices" Examiner quotes the application at page 24, lines 3-4, and page 27, lines 7-8, as stating: "The wafer to be measured ... is resin coated and is ultimately divided into plurality of CSP devices ..." Examiner points to the fact that the application does not state, however what item(s) divides the wafer. Claims 23-27, 42-43 and 46-52 are rejected as depending from the rejected claims. The rejection is respectfully traversed.

The applicant does not understand the alleged lack of clarity. When the wafer is divided, then according to both the claim and the specification, a plurality of semiconductor devices are produced. This is fully consistent with the text of the specification on pages 24 and 27 quoted by the Examiner. "The wafer to be measured 401 is resin coated and is ultimately divided into a plurality of CSP devices 411." Specifically how or with what instrument the wafer is divided is of no real consequence in the present context. It is sufficient to recite a step of "dividing the semiconductor wafer into the plurality of semiconductor devices," as in claim 44. A person of ordinary skill in the art would be knowledgeable about the means available, whether it be a saw or otherwise, for dividing semiconductor wafers into individual devices. For these reasons, it is respectfully submitted that the present claims are in full compliance with the requirements of 35 USC 112, second paragraph, and the rejection, accordingly, should be withdrawn.

The Examiner also rejected claims 21-27 and 42-52 under 35 USC 102(b) as being obvious over *Nakata et al.* (U.S. Patent No. 6,297,658) in view of *Yamamoto* (U.S. Patent No. 6,372,528) The rejection is respectfully traversed.

The present application is a divisional of the applicant's co-pending U.S. Application Serial No. 09/434,490, as specifically referenced in the Preliminary Amendment filed with the present application on July 16, 2001. Therefore, under 35 U.S.C. §120, the present application is entitle to the filing date of its parent, which the Office's records will confirm was November 5, 1999. This date precedes both the U.S. and Japanese filing dates, March 22, 2001 and September 20, 2000, respectively, of the *Yamamoto* reference. Accordingly,

Yamamoto is not available as prior art that can be asserted against the present application.

In the prior Office Action dated April 17, 2002, the *Nakata* reference was applied against the claims. However, the Examiner acknowledges in the present Action that *Nakata* alone does not disclose or suggest all of the limitations of the claimed invention, and relies on *Yamamoto* to cure the deficiencies in *Nakata*. Since *Yamamoto* is not valid prior art, it is respectfully requested that the final rejection of the claims be withdrawn.

Further, all of the Examiner's objections and rejections having been addressed, it is submitted that the application is in condition for allowance. Notice of such, with allowed claims 21-27 and 42-52, is earnestly solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

April 10, 2003
Date

Phillip G. Avruch- Reg. No. 46,076
RABIN & BERDO, P.C.
Telephone: 202-371-8976
Telefax: 202-659-1898
CUSTOMER NO. 23995

PGA:tlc

Appendix

APPENDIX

MARKED-UP CLAIMS

44. (Amended) A method for manufacturing semiconductor devices, the method comprising:

preparing a semiconductor wafer with a first [and] surface and a second surface, the second surface being opposite to the first surface, wherein the first surface has a plurality of circuit elements formed thereon;

forming a plurality of electrodes on the first surface, the electrodes being connected to the circuit elements;

inserting the semiconductor wafer into a burn-in apparatus:

testing the circuit elements in the burn-in apparatus for electrical function, through the electrodes, with the second surface of the semiconductor wafer exposed to convective air in the burn-in apparatus; and

dividing the semiconductor wafer into the plurality of semiconductor devices.